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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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05/30/2006

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EXAMINER

PETRANEK, JACOB ANDREW

ART UNIT

PAPER NUMBER

2183

DATE MAILED: 05/30/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/998,830	Applicant(s) MIYAMOTO, TAIYUU	
	Examiner Jacob Petranek	Art Unit 2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 06 April 2006.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1,2,5,6,8 and 9 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1,2,5,6,8 and 9 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

1. Claims 1-2, 5-6, and 8-9 are pending.
2. The office acknowledges the following papers:
Claims and arguments filed on 4/6/2006.

Withdrawn objections

3. The objection to the title has been withdrawn due to the title amendment.

Maintained Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. §103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

5. Claims 1-2, 5-6, and 8 are rejected under 35 U.S.C. §103(a) as being unpatentable over Sibigroth et al. (U.S. 5,251,304).

6. As per claim 1:

Sibigroth disclosed a microcomputer comprising a memory (Sibigroth: Figure 1 element 13), a central processing unit (Sibigroth: Figure 1 element 14), and a functional block comprising a peripheral block (Sibigroth: Figure 1 element 12), built-in said microcomputer, wherein said memory has a reprogrammable nonvolatile memory (Sibigroth: Column 3 lines 61-67 continued to column 4 lines 1-6), and in which a lock code is written in a specified area (The enable signal provides the lock to a specified

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area.); and the microcomputer comprises:

A first decoding circuit connected with said nonvolatile memory, which reads out said lock code, and decodes said lock code (Sibigtroth: Figure 2 element 50)(The inverter reads out the enable signal and decodes it.);

A logic circuit that performs a predetermined operation on an externally input mode bit, by the output from the first decoding circuit (Sibigtroth: Figure 2 element 52)(The AND gate takes in the decoded enable bit and the instruction fetch bit, which is external to all circuits shown in figure 1, including the instruction inhibit unit.); and

A second decoding circuit that decodes the processed mode bit by receiving the output from said logic circuit, and sends the obtained results to said functional block (Sibigtroth: Figure 2 element 54)(The OR circuit is the second decoding circuit, which decodes the bit output from the AND circuit, and sends its output to the functional block.).

Sibigtroth failed to teach a reprogrammable nonvolatile memory storing user data.

However, Official Notice is given that the reconfigurable nonvolatile memories are well known in the art to store multiple types and instances of important data that needs to be saved even after power is removed from the system. Thus, it would have been obvious to one of ordinary skill in the art at the time the invention to store additional user data in the reprogrammable nonvolatile memory (Programmable Security Device 20) since Official Notice is given that the memories are well known in the art to store multiple types and instances of important data that needs to be saved

even after power is removed from the system.

7. As per claim 2:

Sibigtroth disclosed the microcomputer of claim 1, wherein said logic circuit consists of an AND circuit (Sibigtroth: Figure 2 element 52).

8. As per claim 5:

Sibigtroth disclosed a microcomputer comprising a memory (Sibigtroth: Figure 1 element 13), a central processing unit (Sibigtroth: Figure 1 element 14), a functional block comprising a peripheral block, built-in said microcomputer, and an external terminal (Sibigtroth: Figure 1 elements 12 and 18)(Element 18 receives external signals on external terminals), wherein said memory comprises a reprogrammable nonvolatile memory (Sibigtroth: Column 3 lines 61-67 continued to column 4 lines 1-6), and in which a function-selecting code for selecting the function of the external terminal is written in a specified area (The enable signal is stored within element 20 and is used for selecting a function of the external terminal connecting to elements 18 and 12); and said microcomputer comprises:

A first decoding circuit connected with the nonvolatile memory, which reads out said function-selecting code and decodes this code (Sibigtroth: Figure 2 element 50)(The inverter reads out the enable signal and decodes it.); and

A selector circuit that selects a function of the external terminal by receiving the output from said first decoding circuit (Sibigtroth: Figure 2 element 52, column 3 lines 61-67 continued to column 4 lines 1-32)(The selector circuit (And gate 52) takes decoded enable bit and Instruction Fetch bit, and based on the output of the AND gate

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52, the external terminal (shown in figure 2) performs different functions, i.e., either allowing the bus 30 to connect to the Data bus 24 or not allowing.).

Sibigtroth fails to teach wherein the reprogrammable nonvolatile memory holds user data along with the function selecting code.

However, Official Notice is given that the reconfigurable nonvolatile memories are well known in the art to store multiple types and instances of important data that needs to be saved even after power is removed from the system. Thus, it would have been obvious to one of ordinary skill in the art at the time the invention to store additional user data in the reprogrammable nonvolatile memory (Programmable Security Device 20) since Official Notice is given that the memories are well known in the art to store multiple types and instances of important data that needs to be saved even after power is removed from the system.

9. As per claim 6:

Sibigtroth disclosed a microcomputer comprising a memory (Sibigtroth: Figure 1 element 13), a central processing unit (Sibigtroth: Figure 1 element 14), and a functional block comprising a peripheral block (Sibigtroth: Figure 1 element 12), built-in said microcomputer, wherein said memory comprises a reprogrammable nonvolatile (Sibigtroth: Column 3 lines 61-67 continued to column 4 lines 1-6), and in which a limiting code for limiting a command a memory is written in a specified area (The enable signal provides the lock to a specified area.); and said microcomputer comprises:

A first decoding circuit connected with said nonvolatile memory, which reads out said limiting code, and decodes this code (Sibigtroth: Figure 2 element 50)(The inverter

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reads out the enable signal and decodes it.); and

A second decoding circuit that limits a command to be used, by the output from said first decoding circuit (Sibigtroth: Figure 2 element 54)(The OR circuit is the second decoding circuit, which decodes the bit output from the AND circuit, and sends its output to the functional block.).

However, Official Notice is given that the reconfigurable nonvolatile memories are well known in the art to store multiple types and instances of important data that needs to be saved even after power is removed from the system. Thus, it would have been obvious to one of ordinary skill in the art at the time the invention to store additional user data in the reprogrammable nonvolatile memory (Programmable Security Device 20) since Official Notice is given that the memories are well known in the art to store multiple types and instances of important data that needs to be saved even after power is removed from the system.

10. As per claim 8:

Sibigtroth disclosed the microcomputer of claim 1, wherein said reprogrammable memory consists of a data memory and a program memory (Sibigtroth: Figure 1 element 13, column 3 lines 3-8)(Memory 13, a portion of the memory from claim 1, contains both instructions, data, and is reprogrammable.).

Sibigtroth failed to teach non-volatile memory.

However, Official Notice is given that designing memories as non-volatile allows data and instructions to remain on the disk when the power is removed, and it is well known in the art to design memories as non-volatile for this purpose. Thus, it would

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have been obvious to one of ordinary skill in the art at the time the invention was made to design the memory 13 as non-volatile since Official Notice is given that it is well known to design memories as non-volatile memories so that they can retain data when their power is removed. This would cause the entire memory (memory 13 and Programmable Security Device 20) to be reprogrammable and nonvolatile, and to contain both data and instructions.

11. As per claim 8:

Sibigroth disclosed the microcomputer of claim 1, wherein said reprogrammable nonvolatile memory consists of a data memory and a program memory. (From another point of view than the above rejection of claim 8, While Programmable Security Device is both reprogrammable and nonvolatile (column 3, line 61 to column 4, line 32), it alone does not contain both data and instructions.)

However, Sibigroth suggests the any memory device may be used for Programmable Security Device 20. Thus, it would have been obvious to one of ordinary skill in the art at the time the invention was made to integrate the Programmable Security Device 20 with the Memory 13 since it has been held use of one piece construction instead of the reference structure is matter of obvious engineering choice (In re Larson, 340 F.2d 965, 967, 144 USPQ 347, 349 (CCPA 1965)., and In re Wolfe, 251 F.2d 854, 855, 1 16, USPQ 443, 444 (CCPA 1958)) and since Sibigroth suggests that any memory device can be used to as the Programmable Security Device 20. Integrating the memories would cause there to be one reconfigurable, non-volatile memory that contains both the lock code (data) and other data and instructions.

New Claim Rejections - 35 USC § 103

12. The following is a quotation of 35 U.S.C. §103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

13. Claim 9 is rejected under 35 U.S.C. §103(a) as being unpatentable over Sibigroth et al. (U.S. 5,251,304).

14. As per claim 9:

Sibigroth disclosed the microcomputer of claim 1, wherein the logic circuit masks the input mode bit by the decoded lock code (Sibigroth: Figure 2 element 52)(The selector circuit (And gate 52) takes decoded enable bit and Instruction Fetch bit, and based on the output of the AND gate 52, the external terminal (shown in figure 2) performs different functions, i.e., either allowing the bus 30 to connect to the Data bus 24 or not allowing. The AND circuit provides the mask.).

Conclusion

The following is text cited from 37 CFR 1.111(c): In amending in reply to a rejection of claims in an application or patent under reexamination, the applicant or patent owner must clearly point out the patentable novelty which he or she thinks the claims present in view of the state of the art disclosed by the references cited or the

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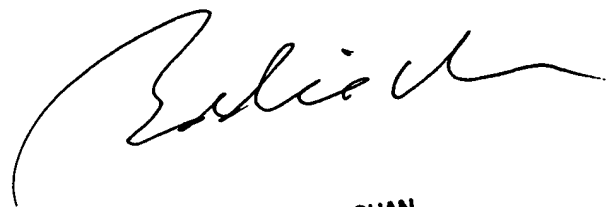
objections made. The applicant or patent owner must also show how the amendments avoid such references or objections.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jacob Petranek whose telephone number is 571-272-5988. The examiner can normally be reached on M-F 8:00-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Jacob Petranek
Examiner
Art Unit 2183



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